IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Jeff C. Morriss	§	Art Unit:	2634
Serial No.:	09/474,359	§		
		§	Examiner:	Kevin Kim
Filed:	December 29, 1999	§		
Title:	Skew Correction Circuit	§	Docket No.	ITL.0294US (P7827)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

Applicant hereby appeals from the Final Rejection dated April 30, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is Intel Corporation, the assignee of the present application by virtue of the assignment recorded at Reel/Frame 010495/0996.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

Date of Deposit: September 26, 2003
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Janice Munoz

III. STATUS OF THE CLAIMS

The application was originally filed with claims 1-19. Claims 20-27, which have been allowed, were added by way of amendment. Claims 1-6, 8-12 and 14-19 have been cancelled, leaving claims 7 and 13 that have been finally rejected and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

An Amendment (copy enclosed) is being filed concurrently with this Appeal Brief requesting the cancellation of claims 8, 9, 12, 14, 15 and 19. Furthermore, in the Amendment, the limitations from dependent claims 8 and 14 have been incorporated into independent claims 7 and 13, respectively. Because 1. the Amendment further narrows the issues on appeal; and 2. no further consideration and/or search by the Examiner is required, it is assumed for purposes of this Appeal Brief that the Amendment will be entered.

V. SUMMARY OF THE INVENTION

Referring to Fig. 4, an embodiment 20 of a skew correction circuit in accordance with the invention measures the amount of delay, or skew, between a data strobe signal and a data signal and delays the strobe signal by approximately the measured amount of skew to minimize the skew between these signals. Due to this arrangement, the skew correction circuit 20 may continually adjust the timing relationship between the data signals and the strobe signal to compensate for skew variation over time that may be attributed to voltage and/or temperature variations. In some embodiments, the skew correction circuit 20 delays the data strobe signal to maintain a quadrature strobing relationship between the data and data strobe signals. Specification, p. 3.

More particularly, in some embodiments, the skew correction circuit 20 receives a data signal (called DATA (see also Fig. 7)) and a data strobe signal (called STROBE (see also Fig. 6)) from lines of a bus. Ideally, the DATA and STROBE signals are aligned in quadrature so that the edges of the STROBE signal are centered in the corresponding data eyes of the DATA signal. However, a delay, or skew 29 (see Fig. 7), may exist between the DATA and STROBE signals, a skew that may cause incorrect data to be captured from the bus. To compensate for this condition, in some embodiments, the skew correction circuit 20 includes logic to combine the data and data strobe signals to produce at least one pulse train signal. As further described below, this pulse train signal has a duty cycle that indicates the degree, or amount, of the skew 29. In this manner, the circuit 20 delays the STROBE signal based on the indication of degree of skew from the

duty cycle to produce a delayed data strobe signal (called D_STROBE), a substantial duplicate of the STROBE signal but shifted in time to remove the skew 29. Specification, pp. 3-4.

To accomplish the skew compensation, in some embodiments, the skew correction circuit 20 includes a quadrature detector 22 (see Fig. 4) that measures the degree, or amount, to which the STROBE signal is not centered with respect to the DATA signal (i.e., the detector 22 measures the skew 29) and provides an error signal (called ERROR (see Fig. 12)) that indicates this measurement and thus, indicates the amount of calibration that is needed. In some embodiments, the ERROR signal is an analog signal that an analog-to-digital converter (ADC) 26 (of the skew correction circuit 20) converts into a digital signal. The skew correction circuit 20 may include an error register 28 that stores an indication called a calibration value, of the digital signal. The calibration value, in turn, is used to directly program the delay by which a programmable delay chain 30 delays the STROBE signal to produce the D_STROBE signal. Therefore, the degree to which the STROBE signal is not centered with respect to the DATA signal establishes the delay that is introduced by the delay chain 30. Specification, p. 4.

Referring to Fig. 5, in some embodiments, the quadrature detector 22 includes logic to combine the DATA and STROBE signals to produce two pulse train signals, each of which has a duty cycle that indicates the degree of skew. In this manner, the quadrature detector may include an XNOR gate 56 that receives the DATA and STROBE signals at different input terminals and produces a signal (called XNOR (see Fig. 9)) whose duty cycle is indicative of the amount of the skew 29. The quadrature detector 22

may also include an XOR gate 58 that receives the DATA and STROBE signals at different input terminals and produces a signal (called XOR (see Fig. 8)) whose duty cycle is indicative of the degree of the skew 29. In general, the duty cycles of the XOR and XNOR signal vary inversely with respect to each other in response to the changes in the skew 29, as described below. The XNOR and XOR signals are received by two low pass filters (LPFs) 60 and 62, respectively, that produce signal that indicate the duty cycles of the received signals. In this manner, the LPF 60 produces a signal (called XNOR_LPF (see Fig. 10)) that indicates the duty cycle of the XNOR signal, and the LPF 62 produces a signal (called XOR_LPF (see Fig. 11)) that indicates the duty cycle of the XOR signal. A differential amplifier 64 (of the skew correction circuit 20) compares the XOR_LPF and XNOR_LPF signals to produce the ERROR signal. Specification, p. 4.

The operation of the quadrature detector 30 is dependent on the transitions of the logical state of the DATA signal and the state of the STROBE signal. In particular, there are four possible combinations of transitions that affect the quadrature detector 30:

1. A logical one to a logical zero transition of the DATA signal when the STROBE signal has a logical one state, as depicted near time T_1 in Figs. 6-12;

2. A logical zero to a logical one transition of the DATA signal when the STROBE signal has a logical one state, as depicted near time T_2 in Figs. 6-12;

3. A logical one to a logical zero transition of the DATA signal when the STROBE signal has a logical zero state, as depicted near time T_3 in Figs. 6-12; and

4. A logical zero to a logical one transition of the DATA signal when the STROBE signal has a logical one state, as depicted near time T_4 in Figs. 6-12; Specification, p. 5.

For transition numbers one and two, the duty cycle of the XOR signal and the level of the XOR_LPF signal decreases with an increase in the skew 29, and the duty cycle of the XNOR signal and the level of the XNOR_LPF signal increases with an increase in the skew 29. This relationship causes the ERROR signal to indicate a positive value that is proportional to the degree of skew, as depicted in Fig. 12. Specification, p. 5.

For transition numbers three and four, the duty cycle of the XOR signal and the level of the XOR_LPF signal increases with an increase in the skew 29, and the duty cycle of the XNOR signal and the level of the XNOR_LPF signal decreases with an increase in the skew 29. This relationship causes the ERROR signal to indicate a negative value that is proportional to the degree of skew, as depicted in Fig. 12. Specification, p. 5.

Therefore, using these relationships, in some embodiments, a calibration data pattern may be used to produce a net error offset (as indicated by the ERROR signal) whenever there is a nonzero quadrature error. In some embodiments, the calibration data pattern is chosen to implement either transitions one and two or transitions three and four, without mixing these groupings. Specification, p. 5.

The LPFs 56 and 58 (see Fig. 5) of the quadrature detector 20 filter out frequency components (of the XOR and XNOR signals) that are a function of the data rate and the

edge rate to produce the XOR_LPF and XNOR_LPF signals that are nearly DC. Any non-DC components of the XOR_LPF and XNOR_LPF signals are attributable to the variance of the skew with voltage and temperature. Typically, the component of the skew that varies in such a manner that this variation has a maximum bandwidth of 10Hz or less. Besides producing newly DC signals, the LPFs 56 and 58 also provide bandlimiting for purposes of preventing the ADC 26 from receiving a signal that has a frequency greater than one half of the sampling frequency of the sample-and-hold circuit 24. As an example, the ADC 26 may be a delta-sigma ADC. Other ADCs may be used in other embodiments. Specification, pp. 5-6.

The calibration value is stored in the error register 28 each time the quadrature error is updated, and the rate at which the error register 28 is updated is a function of how rapidly the skew can change. If the skew exhibits little change over time then it may be sufficient to update the error register 28 only at power-up. Otherwise the error register 28 may be updated at a rate slightly faster than the skew can change. In some embodiments, a control unit 25 controls when updates to the error register 28 are made. Specification, p. 6.

In some embodiments, the delay chain 30 may include inverters that are coupled together via multiplexers to form the desired delay. The delay chain 30 is designed for the appropriate dynamic range and resolution. In this manner, because in some embodiments, coincident strobing may be used at the source, the dynamic range accommodates the delay of one half of the bit time plus maximum amount of skew that needs to be corrected. The resolution specifies how fine a correction can be made.

Typically the resolution should be on the order of the setup, or hold, time for the receive buffer. For example, for current silicon processes this is about 50 picoseconds (pS). However, this value may be reduced or increased according to the particular process. Specification, p. 6.

As an example, a 500 megabits per second (Mb/s) system may have up to +/-500 pS of skew. The bit time for this system is 2.0 nanoseconds (nS), so that one half of a bit time would be 1.0 nS. For this example, the delay chain 30 may be designed to delay a nominal 1.0 nS (to center the strobe if there were no other skew) plus an additional delay of 500pS (to account for worst case skew). The normal operating range of the delay would then be 500 pS - 1.5 nS. Specification, p. 6.

Referring to Fig. 13, in some embodiments, a skew correction circuit 20 may be associated with each data line 23 of the bus. In this manner, this arrangement accommodates different skews between each different data signal and the data strobe signal. Each skew correction circuit 20 is coupled between a different one of the data lines 23 and the associated data output line 27. Specification, p. 6.

Other arrangements are within the scope of the following claims. For example, Fig. 14 depicts a receiver 100 that includes multiplexing features to minimize the number of skew correction circuits. In this manner, the skew correction circuit 100 provides multiple strobe signals (called STB_0, . . . STB_i), each of which is associated with one of the data lines 23 and may be used to compensate a different skew. In this manner, the skew correction circuit includes a quadrature detector 110 and an ADC 112 that function similar the quadrature detector 22 and the ADC 26 of the skew correction circuit 20. The

output terminals of the ADC 112 are coupled to error registers 114. Each error register 114, in turn, is associated with a different data line 23 and stores an indication of the delay to be used with the strobe signal that is associated with the data line 23. In this manner, the output terminals of each error register 114 are coupled to the select terminals of a different multiplexer 118, and the input terminals of each multiplexer 118 are coupled to taps of a delay chain 116 that receives a buffered strobe signal. The output terminal of each multiplexer 118 is coupled to the clock input of a different data bit receive buffer that may be formed from a D-type flip-flop, for example. Due to this arrangement, the indication that is stored in a particular error register 114 causes the associated multiplexer 118 to select the appropriate tap of the delay chain 116 and thus, select the appropriate strobe delay. Thus, the skew correction circuit 110 is capable of correcting the skew that is associated with each data line 23. Specification, p. 7.

For purposes of storing the appropriate indications of the error registers 114, the skew correction circuit includes a multiplexer 124 that has input terminals that are coupled to the output terminals of the multiplexers 118, and the output terminal of the multiplexer 124 is coupled to an input terminal of the quadrature detector 110. The other input terminal of the quadrature multiplexer 110 is coupled to the output terminal of a multiplexer 102. The input terminals of the multiplexer 110, in turn, are coupled to the data lines 23. A controller 120 of the skew correction circuit 100 is coupled to the selection terminals of the multiplexers 102 and 118 and to the error registers 114 so that the controller 120 may selectively measure the skews that are associated with each of the

data lines 23 and cause an indication of the measured skew to be stored in the appropriate error register 114. Specification, p. 7.

Among the other features of the skew correction circuit 100, the circuit 100 may include matched delay elements 102, each of which is coupled between a different one of the data lines 23 and the input terminal of a different one of the D-type flip-flops 106. The skew correction circuit 100 may also include matched delay elements 122, each of which is coupled between the clock input terminal of a different D-type flip-flop 106 and a different one of the output terminals of the multiplexer 118. Specification, pp. 7-8.

VI. ISSUES

A. Can claim 7 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness?

B. Can claim 13 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness?

VII. GROUPING OF THE CLAIMS

Claims 7 and 13 are each separately patentable for the reasons set forth below. Thus, regardless of the grouping that is set forth by the Examiner's rejections, claims 7 and 13 stand alone with respect to each other and do not stand or fall together.

VIII. ARGUMENT

All claims should be allowed over the cited references for the reasons set forth below.

A. Can claim 7 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness?

The data receiver of claim 7 includes buffers, a first circuit, a second circuit and registers. Each buffer latches a different data bit signal. The first circuit, for each data signal, generates at least one associated pulse train signal in response to a strobe signal and the data bit signal. A duty cycle of the associated pulse train signal(s) indicate a degree of skew between the associated data bit signal and the strobe signal. The second circuit is coupled to the first circuit and the buffers to regulate latching of the data bit signals by the buffers based on the indicated degrees of skew. Each register is associated with a different one of the data bit signals and indicates the degree of skew between the strobe signal and the associated data bit signal.

As stated above in Section IV above, the Amendment that is being concurrently filed with the Appeal Brief incorporates the limitations of dependent claim 8 into independent claim 7. Therefore, the Examiner's rejection of claim 8 is addressed below.

The Examiner rejected claim 8 under 35 U.S.C. § 103(a) as being obvious in view of the combination of U.S. Patent No. 6,247,138 B1 (hereinafter called "Tamura"), U.S. Patent No. 5,736,872 (hereinafter called "Sharma"); and U.S. Patent No. 5,973,526 (hereinafter called "Dabral"). However, as set forth below, this combination fails to teach or suggest all limitations of claim 8, and for at least this reason, a *prima facie* case of obviousness has not been established for this claim.

Tamura teaches various circuits of a semiconductor integrated circuit. Among these circuits are two different and distinct circuits that perform entirely different functions: a timing signal generating circuit and a timing adjusting circuit. Tamura discusses various embodiments

of both of these circuits. As an example, an embodiment of the timing signal generating circuit is depicted in Figure 2 of Tamura. As discussed in lines 66-67 of column 13 and in lines 1-8 in column 14 of Tamura, the timing signal generating circuit counts clock phases and generates control signals for purposes of operating a DRAM core. A more specific embodiment of the timing signal generating circuit is depicted in Figure 44 of Tamura. As can be seen from Figure 44, the timing signal generating circuit includes a phase comparator 312 that receives clock signals and generates corresponding up and down signals to control the generation of timing signals. Tamura also describes the circuitry depicted in Figure 52 as being another embodiment of the timing signal generating circuit. As depicted in Figure 52, the timing signal generator in this embodiment includes a phase comparator 312 that is connected to an up-down counter 134.

As mentioned above, another circuit described in Tamura is a timing adjusting circuit. The timing adjusting circuit is separate from and performs an entirely different function than the timing signal generating circuit described above. In contrast to the timing signal generating circuit, Tamura's timing adjusting circuit adjusts a relative timing relationship between a received data signal and a clock signal. Tamura, 19:26-32. Although Tamura discusses many embodiments of the timing adjusting circuit, by way of example, one embodiment of the timing adjusting circuit is depicted in Figure 14 of Tamura.

Sharma generally describes a phase frequency detector. In the § 103 rejection, the Examiner relies on the following language from Sharma:

> All phase detectors, of whatever design, are intended to produce an output signal proportional in magnitude or duty cycle to the phase difference between their two input signals.

Sharma, 6:25-27.

Dabral generally teaches locked loop circuits to compensate clock signals. In this compensation scheme, Dabral discloses a phase comparator 48 that generates an up-down signal to control a charge pump 50, as depicted in Figure 5 of Dabral.

In the § 103 rejection of claim 8, the Examiner contends that the up-down counter depicted in Fig. 52 of Tamura discloses the registers of claim 8. Final Office Action, 4. However, as discussed above, Fig. 52 of Tamura discusses a timing signal generating circuit, a circuit that controls signals in response to a clock signal. Neither the timing signal generating circuit of Figure 52, nor any of the other timing signal generating circuits disclosed in Tamura, contain circuitry that indicate a degree of skew between a strobe signal and an associated data bit signal, as the up-down counters do not process any signal relative to the skew of a data bit signal.

It appears the Examiner is confusing Tamura's discussion of timing adjusting circuits (such as the circuit in Fig. 14) with Tamura's discussion timing signal generating circuits. However, these are two distinct circuits in Tamura and are used for entirely different purposes. Therefore, neither the up-down counter nor any of circuitry of Fig. 52 indicates the degree of skew between the strobe signal and the associated data bit signal, as the circuitry in Fig. 52 does not detect or otherwise receive such an indication.

Thus, referring to the relevant circuitry of Tamura, Tamura neither teaches nor suggests such registers for use with the timing adjusting circuits, such as the circuit depicted in Fig. 14. In fact, Tamura is silent regarding the output from the phase comparator of the timing adjust circuits, such as the phase comparator 5301 depicted in Figure 14 of Tamura.

Thus, Tamura fails to teach or even suggest the registers of claim 8. Furthermore, neither Sharma nor Dabral teaches or suggests the missing claim limitations. Therefore, as the

combination of references fails to teach or suggest all claim limitations, the Examiner has failed to establish a *prima facie* case of obviousness for claim 8 for at least this reason.

The Examiner failed to establish a *prima facie* case of obviousness for claim 8 for the additional, independent reason that the Examiner shows no support for the alleged suggestion or motivation to combine any of the three references together. Such a suggestion or motivation in the prior art must be specifically pointed out by the Examiner to establish a *prima facie* case of obviousness. *See Ex parte Gambogi*, 62 USPQ2d 1209, 1212 (Bd. Pat. App. & Int. 2001); *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P. § 2143. "Obviousness cannot be predicated on what is unknown." For a *prima facie* case of obviousness, the Examiner must support the alleged suggestion or motivation with a specific cite to some portion of a cited reference, as "obviousness cannot be predicated on what is unknown." *In re Spormann*, 363 F.2d 444, 448, 150 USPQ 449, 452 (CCPA 1966).

Thus, the § 103 rejection of claim 8 (now rewritten in independent form as claim 7) is improper and should be reversed.

B. Can claim 13 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness?

The method of claim 13 includes using a data bit signal and a first strobe signal to generate at least one pulse train signal. A duty cycle of the pulse train signal(s) indicates a degree of skew between the data bit signal and the first strobe signal. The method includes regulating a timing relationship between the data bit signal and a second strobe signal based on

the degree of skew indicated by the duty cycle. The method also includes storing a calibration value indicative of the degree of skew.

The limitations of claim 14 have been incorporated into claim 13. Therefore, the Examiner's rejection of claim 14 is addressed below.

The Examiner rejected claim 14 under 35 U.S.C. § 103(a) as being obvious in view of the combination of Tamura, Sharma and Dabral. However, the Examiner fails to establish a *prima facie* case of obviousness for claim 14 for at least the reason that the combination of references fails to teach or suggest all claim limitations. For example, none of the cited references teach or suggest storing a calibration value that is indicative of a degree of skew.

The Examiner relies on Tamura for the alleged teaching of storing a calibration value indicative of a degree of skew. In particular, the Examiner refers to a counter of a timing signal generating circuit in Figure 52 of Tamura. However, the timing signal generating circuit is in no way related to a circuit that adjusts or compensates for a degree of skew. Instead, the Examiner is selectively reading Tamura and confusing Tamura's discussion of a timing adjusting circuit (a circuit that adjusts a timing relationship between a data signal and a clock signal) and Tamura's discussion of a timing signal generating circuit, a circuit that generates control signals based on clock signals only. To summarize, Tamura neither teaches nor suggests the storing of claim 14.

Thus, the Examiner fails to establish a *prima facie* case of obviousness for claim 14 for at least the reason that the combination of references fails to teach or suggest all claim limitations. The Examiner also fails to establish a *prima facie* case of obviousness for claim 14 for at least the additional, independent reason that the Examiner fails to show where the prior art contains the alleged suggestion or motivation to combine Tamura, Sharma and Dabral. In this manner,

the Examiner does not provide any specific support showing the alleged suggestion or motivation for the combination of any of these references. This is improper, however, as the Examiner must point out where the prior art contains such an alleged suggestion or motivation. *See Ex parte Gambogi*, 62 USPQ2d 1209, 1212 (Bd. Pat. App. & Int. 2001); *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P. § 2143.

Thus, the Examiner's rejection of claim 14 (now rewritten in independent form as claim 13) is improper and should be reversed.

IX. CONCLUSION

Applicant requests that each of the final rejections be reversed and that the claims subject to this appeal be allowed to issue.

Respectfully submitted,

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APPENDIX OF CLAIMS

The claims on appeal are:

7. A data receiver comprising:

buffers, each buffer to latch a different data bit signal;

a first circuit to:

for each data signal, generate at least one associated pulse train signal in response to a strobe signal and the data bit signal, a duty cycle of said at least one associated pulse train signal indicating a degree of skew between the associated data bit signal and the strobe signal; and

a second circuit coupled to the first circuit and the buffers to regulate latching of the data bit signals by the buffers based on the indicated degrees of skew,

wherein the first circuit comprises registers, each register being associated with a different one of the data bit signals and indicating the degree of skew between the strobe signal and the associated data bit signal.

13. A method comprising:

using a data bit signal and a first strobe signal to generate at least one pulse train signal, a duty cycle of said at least one pulse train signal indicating a degree of skew between the data bit signal and the first strobe signal;

regulating a timing relationship between the data bit signal and a second strobe signal based on the degree of skew indicated by the duty cycle; and

storing a calibration value indicative of the degree of skew.